REMARKS

Claims 1-4, 8-54 and 58-72 are rejected under 35 U.S.C. 102(e) as being anticipated by Ollivier, *et al.* (U.S. Patent Number 6,738,881). Claims 5-7 and 55-57 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ollivier, *et al.* In view of the amendments to the claims and the following remarks, the rejections are respectfully traversed, and reconsideration of the rejections is requested.

In the present invention as claimed in claims 1-22, a system for transferring a signal to a channel includes a storage unit associated with the channel for storing source identification information of a plurality of sources and indicating an order of priority of the plurality of sources for access to the channel. The system further includes a plurality of selection circuits for receiving input signals from the sources, each of the selection circuits selecting one of the plurality of input signals. The system further includes a circuit for checking outputs of the selection circuits and forwarding selected input signals to the channel, such that the selected input signals are forwarded to the channel according to the priorities associated with the sources.

In the present invention as claimed in claims 23-36, a system for transferring signals to channels includes a plurality of storage units, each storage unit being associated with one of the channels, and each storage unit being adapted to store source identification information for each of the sources that can transfer input signals to the associated channel and indicating an order of priority of the sources for access to the channel. The system further includes a plurality of selection circuits for receiving input signals from the sources, each of the selection circuits selecting one of the plurality of input signals. The system further includes a circuit for checking outputs of the selection circuits and forwarding selected input signals to the channel, such that the signals are forwarded to the channels according to the priorities associated with the sources.

In the present invention as claimed in claims 37-50, a direct memory access (DMA) controller for controlling transfer of signals from input sources to output devices, a plurality of channels being connected to the output devices, includes a plurality of storage units, each storage unit being associated with one of the channels, and each

storage unit being adapted to store source identification information for each of the sources that can transfer input signals to the associated channel and indicating an order of priority of the sources for access to the channel. The system further includes a plurality of selection circuits for receiving input signals from the sources, each of the selection circuits selecting one of the plurality of input signals. The system further includes a circuit for checking outputs of the selection circuits and forwarding selected input signals to the channel, such that the signals are forwarded to the channels according to the priorities associated with the sources.

In the present invention as claimed in claims 51-72, a method of transferring a signal to a channel includes storing source identification information for a plurality of sources and indicating an order of priority of the plurality of sources for access to the channel in a storage unit associated with the channel. The method further includes providing a plurality of selection circuits for receiving input signals from the sources, each of the selection circuits selecting one of the plurality of input signals. The method further includes, with a checking circuit, checking outputs of the selection circuits and forwarding a selected input signal to the channel, such that the signal is forwarded to the channel according to the priorities associated with the sources.

In the present invention as claimed, a storage unit is associated with each channel. Source identifiers which identify sources that may use a channel are stored in the register associated with the channel according to the priory of the associated sources. Each of a plurality of selection circuits selectively passes on the plurality of input signals from a respective one of the plurality of sources based on the source identification information of a source associated with the selection circuit.

Ollivier, *et al.* discloses that a scheduler scans all the channel descriptor registers (a source descriptor 650, a destination descriptor 652 and enable descriptor 620) and FIFO counters to determine if requests are waiting to be served. Each possible request is given a request identifier. If there are several requests waiting, they are served on a round robin scheme. If request r is the current request served, the next request served will be r+1.

Ollivier, *et al.* fails to teach or suggest a system for transferring a signal to a channel which includes a storage unit associated with the channel for storing source identification information of a plurality of sources and indicating an order of priority of

the plurality of sources for access to the channel, and a circuit for checking outputs of the selection circuits and forwarding selected input signals to the channel, such that the signal is forwarded to the channel according to the priorities associated with the sources, as claimed in claims 1-22. In addition, Ollivier, *et al.* fails to teach or suggest a system for transferring signals to channels includes a plurality of storage units, each storage unit being associated with one of the channels, and each storage unit being adapted to store source identification information for each of the sources that can transfer input signals to the associated channel and indicating an order of priority of the sources for access to the channel, and a circuit for checking outputs of the selection circuits and forwarding selected input signals to the channel, such that the signals are forwarded to the channels according to the priorities associated with the sources, as claimed in claims 23-36. Further, Ollivier, *et al.* fails to teach or suggest a direct memory access (DMA) controller that includes a plurality of storage units, each storage unit being associated with one of the channels, and each storage unit being adapted to store source identification information for each of the sources that can transfer input signals to the associated channel and indicating an order of priority of the sources for access to the channel, and a circuit for checking outputs of the selection circuits and forwarding selected input signals to the channel, such that the signals are forwarded to the channels according to the priorities associated with the sources, as claimed in claims 37-50. In addition, Ollivier, *et al.* fails to teach or suggest a method of transferring a signal to a channel which includes storing source identification information for a plurality of sources and indicating an order of priority of the plurality of sources for access to the channel in a storage unit associated with the channel, and, with a checking circuit, checking outputs of the selection circuits and forwarding a selected input signal to the channel, such that the signal is forwarded to the channel according to the priorities associated with the sources, as claimed in claims 51-72.

The Office Action indicates at page 15, section 43, that in Ollivier, *et al.* each channel descriptor, i.e. source descriptor 650, destination descriptor 652 and enable descriptor 654, "stores identification as source descriptor 650, destination descriptor 652 and enable descriptor 654". In Ollivier, *et al.*, the source descriptor indicates a source of the transfer, the destination descriptor indicates a destination of the transfer, and the enable descriptor indicates whether the channel is enabled or disabled. In determining

which request to serve, the channel descriptors are merely scanned in order to determine if requests are waiting to be served. The requests in Ollivier, *et al.* are given identifiers and then are served based on a round robin scheme. The source descriptor 650, the destination register 652 and the enable descriptor 654 of Ollivier, *et al.* in no way indicate an order of priority of the plurality of sources for access to the channel. The source information in the channel descriptors of Ollivier, *et al.* is in no way used in determining a priority of sources. The source descriptor 650, the destination register 652 and the enable descriptor 654 of Ollivier, *et al.* merely indicate whether requests are waiting to be served. Therefore, it is believed that Ollivier, *et al.* in no way teaches or suggests a storage unit associated with a channel indicating an order of priority of the plurality of sources for access to the channel, as claimed.

The Office Action further indicates that, in Ollivier, *et al.*, "schedulers may use the enable/disable priority algorithm for specific ports where the channel priority field are overlaid onto the round-robin scheme allowing transfer of high priority channels over low priority channels." In Ollivier, *et al.*, the channel priority PRIO(5:0) field defines the priority of each channel. PRIO[i]=0 indicates channel i has a low priority; PRIO[i]=1 indicates channel i has a high priority. A HPI priority HPI[1:0] field defines the priority of the host port in relation to the DMA channels. In a given round-robin queue, each channel is switched to the next channel after its read has been triggered. The low priority channels will be pending as long as high priority channels need to be triggered. The channel priorities refer to the priorities of the channels, not an order of priorities of the plurality of sources for access to the channel. Therefore, it is believed that Ollivier, *et al.* in no way teaches or suggests a storage unit associated with a channel indicating an order of priority of the plurality of sources for access to the channel, as claimed. Therefore, it is believed that Ollivier, *et al.* in no way teaches or suggests a storage unit associated with a channel indicating an order of priority of the plurality of sources for access to the channel, as claimed.

Ollivier fails to teach or suggest certain elements of the invention set forth in claims 1-22, 23-36, 37-50 and 51-72, as discussed above. Therefore, it is believed that the amended claims are allowable over the cited reference, and reconsideration of the rejections of claims 1-4, 8-54 and 58-72 under 35 U.S.C. 102(e) as being anticipated by

Ollivier, *et al.*, and the rejections of claims 5-7 and 55-57 under 35 U.S.C. § 103(a) based on Ollivier, *et al.* is respectfully requested.

In view of the foregoing remarks, it is believed that, upon entry of this Response, all claims pending in the application will be in condition for allowance. Therefore, it is requested that this Response be entered and that the case be allowed and passed to issue. If a telephone conference will expedite prosecution of the application, the Examiner is invited to telephone the undersigned.

In connection with this matter, please charge any otherwise unpaid fees which may be due or credit any overpayment to Deposit Account No. 501798.

Respectfully submitted,

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